Review research
https://doi.org/10.31854/1813-324X-2025-11-5-42-59
EDN:WXEIHS

LDPC and Polar Codes in 6G: A Comparative Study and Unified Frameworks

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Annotation

Relevance. *As sixth-generation (6G) wireless systems pursue extreme requirements in throughput, latency, reliability, and adaptability, the design of channel coding schemes becomes increasingly critical. This paper presents a comprehensive comparison between Low-Density Parity-Check (LDPC) codes and Polar codes, the two most promising channel coding candidates for 6G. We analyze their respective strengths across key metrics including data throughput, error-correction capability, decoding complexity, hardware implementation, and adaptability to dynamic communication scenarios. Furthermore, we explore recent advances in unified channel coding frameworks, including generalized LDPC with Polar-like components (GLDPC-PC) and artificial intelligence (AI)-assisted decoders, which aim to bridge the performance gap across diverse 6G scenarios.*

Purpose. *This paper aims to provide a systematic and measurable comparison of LDPC and Polar codes for 6G, while also examining the feasibility of unified coding frameworks to bridge their performance gaps.*

Methods used. *This study employs a systematic literature review. The analysis first evaluates LDPC and Polar codes against four key metrics: data throughput, error-correction capability, decoding complexity and hardware implementation, and flexibility. It then examines advancements in long- and short-block code design and unified frameworks. The comparison is substantiated by a quantitative analysis of documented performance data.*

Results. *LDPC codes demonstrate strong hardware scalability and parallelism, while Polar codes excel in short-packet error correction. Unified approaches integrate their advantages, enhancing adaptability to diverse scenarios.*

Novelty. *Unlike prior works with fragmented analyses, this study combines comparative evaluation with an exploration of unified frameworks, providing an integrated perspective.*

Theoretical significance. *The results enrich theoretical understanding of 6G coding trade-offs. The paper offers a guidance for researchers and standardization bodies in designing future coding strategies.*

Practical significance. *The practical significance of the work lies in the fact that the conducted comparative study of LDPC and Polar codes enables a well-founded selection of channel coding schemes for various 6G communication scenarios. The obtained results can be used in the design of 6G communication systems to optimize the choice between codes: Polar codes are suitable for short packets requiring low latency and high energy efficiency, while LDPC codes (particularly SC-LDPC) are ideal for long codes where hardware scalability and parallelism are critical. The results are also applicable to the development of unified decoders and adaptive systems capable of dynamically switching between schemes, which enhances the flexibility and efficiency of future telecommunication infrastructures.*

Keywords: *6G, channel coding, LDPC codes, Polar codes*

Funding: *The research was supported by RSF (project 25-29-00139), https://rscf.ru/roject/25-29-00139 in TUSUR.*

For citation: Zhang W., Gazizov T.R. LDPC and Polar Codes in 6G: A Comparative Study and Unified Frameworks. *Proceedings of Telecommunication Universities.* 2025;11(5):42–59. DOI:10.31854/1813-324X-2025-11-5-42-59. EDN:WXEIHS

Обзорная статья
УДК 004.7+004.738.2: 004.738.5
https://doi.org/10.31854/1813-324X-2025-11-5-42-59
EDN:WXEIHS

LDPC и полярные коды в 6G: сравнительное исследование и унифицированные фреймворки

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Аннотация

Актуальность. *По мере того, как беспроводные системы 6G стремятся удовлетворить экстремальные требования к пропускной способности, задержке, надежности и адаптивности, проектирование схем канального кодирования приобретает все более критическое значение. В данной статье представлен всесторонний сравнительный анализ кодов с малой плотностью проверок на четность (LDPC) и полярных кодов – двух наиболее перспективных кандидатов на роль канальных кодов для 6G. Рассматриваются их сильные стороны по ключевым метрикам, включая пропускную способность передачи данных, помехоустойчивость, сложность декодирования, аппаратную реализацию и адаптивность к динамичным условиям связи. Кроме того, обсуждаются современные подходы к созданию унифицированных фреймворков канального кодирования, включая обобщенные коды LDPC с компонентами, аналогичными полярным, и декодеры, основанные на искусственном интеллекте, направленные на сокращение разрыва в производительности в различных сценариях 6G.* ***Целью*** *данной работы является проведение систематического и измеримого сравнения LDPC и полярных кодов для 6G, а также изучение возможностей унифицированных кодовых структур для преодоления их разрыва в производительности.*

Используемые методы. *В данном исследовании применяется систематический обзор литературы. Анализ начинается с оценки кодов LDPC и полярных кодов по четырем ключевым метрикам: пропускная способность, помехоустойчивость, сложность декодирования и аппаратная реализация, а также гибкость. Затем рассматриваются достижения в области проектирования длинных и коротких блочных кодов, а также унифицированные фреймворки. Сравнение подкреплено количественным анализом документированных данных о производительности.*

Результаты. *Коды LDPC демонстрируют высокую масштабируемость и возможность параллельной аппаратной реализации, тогда как полярные коды показывают преимущества в коррекции ошибок при коротких блоках. Унифицированные подходы позволяют объединить их сильные стороны, повышая адаптивность к различным сценариям.*

Новизна. *В отличие от предыдущих работ с фрагментарным анализом, данное исследование объединяет сравнительную оценку с рассмотрением унифицированных подходов, формируя целостное представление.*

Теоретическая значимость. *Результаты обогащают теоретическое понимание компромиссов при выборе кодов для 6G и расширяют знания о перспективах их развития. Работа предлагает прикладные ориентиры для исследователей и органов стандартизации при разработке стратегий построения кодовых схем следующего поколения.*

Практическая значимость. *Полученные результаты могут быть использованы при проектировании систем связи 6G для оптимизации выбора между кодами: полярные коды – для коротких пакетов с требованиями низкой задержки и высокой энергоэффективности; LDPC (в частности, SC-LDPC) – для длинных кодов, где критичны аппаратная масштабируемость и распараллеливание. Результаты также применимы для разработки унифицированных декодеров и адаптивных систем, динамически переключающихся между схемами, что повышает гибкость и эффективность телекоммуникационных инфраструктур.*

Ключевые слова: *6G, канальное кодирование, LDPC-коды, полярные коды*

Финансирование: *Исследование поддержано РНФ (проект 25-29-00139), https://rscf.ru/roject/25-29-00139 в ТУСУРе.*

Ссылка для цитирования: Чжан В., Газизов Т.Р. A Comparative Study and Unified Frameworks // Труды учебных заведений связи. 2025. Т. 11. № 5. С. 42–59. DOI:10.31854/1813-324X-2025-11-5-42-59. EDN:WXEIHS

Introduction

Channel coding adds structured redundancy to transmitted signals, enabling robust error correction against noise, interference, and channel fading, thereby ensuring data integrity at the receiver side [1]. It is fundamental to maintaining both transmission reliability and user experience in modern wireless communication systems. Compared with the fifth-generation (5G) networks, sixth-generation (6G) communications aim to deliver significantly higher throughput, ultra-low latency, high accuracy and flexibility [2, 3]. These ambitious goals impose unprecedented demands on forward error correction (FEC) schemes in terms of decoding efficiency, flexibility, and hardware scalability.

Current mainstream channel coding techniques include Turbo codes, Low-Density Parity-Check (LDPC) codes, and Polar codes. Turbo codes provide excellent error correction performance but depend on iterative decoding with limited parallelism capabilities, resulting in high latency and reduced scalability. These characteristics make them less favorable for core 6G scenarios that demand ultra-low latency and extremely high data throughput [4, 5]. In contrast, LDPC and Polar codes have already been adopted in global wireless standards due to their capacity-approaching performance and favorable decoding characteristics [1]. Both are theoretically capable of approaching the Shannon limit and are better aligned with the stringent KPIs of 6G communications. However, given the complexity and diversity of future 6G scenarios, there remains a critical need for comprehensive evaluation and comparative analysis of these two coding paradigms to guide optimal coding scheme selection.

Although several studies have provided comprehensive analyses of channel coding schemes for 6G [6–8], most remain limited to qualitative descriptions of the fundamental characteristics and trade-offs of LDPC and Polar codes. While some recent works have highlighted individual advancements in these codes, a systematic comparison under key 6G performance metrics is still lacking – particularly regarding their adaptability to both long and short block length scenarios. Furthermore, the feasibility and design path of a unified channel coding framework for 6G have yet to be thoroughly investigated.

This paper presents a systematic and in-depth analysis of the recent developments of LDPC and Polar codes in the context of 6G. We begin by examining their fundamental code structures and decoding architectures. Then we compare their advancements across 4 key dimensions: data throughput, error correction performance, decoding complexity and hardware implementation, and flexibility and adaptability. Furthermore, we analyzed the development trends of long and short block codes in 6G communication systems and summarized the current key technological approaches and representative research achievements. Finally, we explore the evolution and representative approaches of unified channel coding frameworks. Our objective is to clarify the design trade-offs and potential synergies between these two coding paradigms, providing valuable insights for the design of next-generation channel coding strategies in 6G.

Fundamentals of LDPC and Polar Codes

LDPC codes, as one of the FEC codes with excellent performance, are also a hot spot area for 6G channel coding. LDPC codes are a class of linear block codes with sparse check matrices, which were first proposed in [9]. The LDPC code can be determined by the check matrix **H**, which is a sparse matrix of size $m \times n$ where m is the length of the check bits, n is the length of the LDPC code, the length of the information bits is $k = n - m$, and the code rate is $R = k / n$. The structure of LDPC codes is flexible, primarily determined by the design of the **H** matrix. By adjusting the number of rows and columns in the **H** matrix, both the code rate and code length can be flexibly controlled. The construction methods of the LDPC code's **H** matrix can be broadly categorized into random construction and structured construction, each with its own advantages and disadvantages. **H** matrices generated through random construction can theoretically approach the Shannon limit, but their irregular structure leads to complex hardware implementation and makes it difficult to optimize the decoder for parallel processing [9, 10]. In contrast, **H** matrices generated through structured construction are hardware friendly and support efficient parallel decoding, but their performance is inferior to that of optimally constructed random LDPC codes [11, 12].

In order to more intuitively show the sparse connection relationship between the information bit (variable node) and the check bit (check node) in the **H** matrix, and to identify the local structural features of the **H** matrix, the **H** matrix can be represented by a Tanner graph [13]. The 6 columns and 4 rows check matrix **H** of a LDPC code, along with its corresponding Tanner graph is illustrated in Fig. 1. In the Tanner graph, a closed loop starting from a node and returning to the starting point after passing through several edges without repeating the path is called a cycle. The red line in Fig. 1 shows a circle with a girth of 6. The girth will directly affect the performance of the LDPC codes decoding algorithms. Short cycles limit the independence between nodes, causing local errors to propagate rapidly through the cyclic structure. This causes the BER of the decoding algorithm to stagnate at high SNR, resulting in an error floor. To improve the reliability and efficiency of LDPC

codes, designers commonly avoid 4-cycles and target girth ≥ 6; in modern standards such as 5G NR and Wi-Fi 6 [14].

LDPC codes decoding relies on an iterative process that involves exchanging messages between the VNs and CNs in the Tanner graph [13]. At current, soft decision algorithm is the mainstream algorithm of LDPC codes decoding algorithm, and the BP decoding algorithm, which is closest to the channel capacity, is the soft decision decoding algorithm [15].

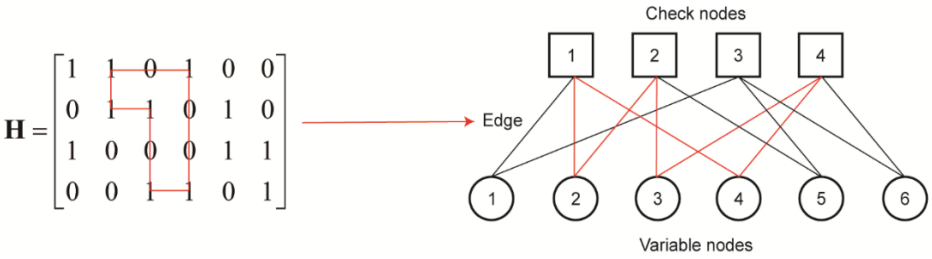

*Fig. 1. **H** Matrix of LDPC Code with 6 Columns and 4 Rows and the Corresponding Tanner Graph*

The soft decision algorithm is based on probability theory in which the message passed is the probability value associated with the occurrence of a particular bit. Fig. 2 illustrates a typical computational model of a soft verdict decoding algorithm, where the original posteriori probabilities are first input to the VNs, and then the information is iterated between the VNs and CNs. Soft decision decoding algorithms also include LLR-BP, MS, and so on.

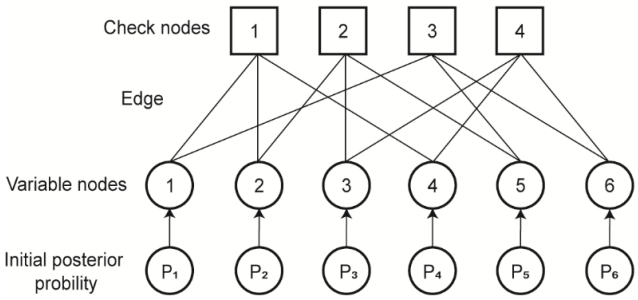

Fig. 2. Soft Decision Algorithm Typical Computational Model

As the length of LDPC codes increases, the parity check matrix becomes larger while maintaining low density, resulting in longer cycles in the Tanner graph and reducing the impact of short cycles. Meanwhile, in the sparse matrix of long LDPC codes, the large number of nodes and sparse connections allow messages to propagate through multiple independent paths during the iterative process. The independent information from these paths complements each other, enabling the decoding algorithm to cross verify errors from multiple perspectives in each iteration, leading to significantly improved error correction performance [9, 16]. Therefore, LDPC codes are particularly well suited for transmission schemes involving long code blocks. For instance, 5G NR supports a maximum code length of up to 8448 bits, which provides favorable conditions for LDPC codes to achieve highly parallel decoding and near Shannon limit performance, allowing their advantages to be fully realized (https://portal.3gpp.org/ngppapp/CreateTdoc).

Polar codes have been rigorously proven to achieve the Shannon capacity. The core structure of Polar codes is processed by channel polarization [17]. Channel polarization includes two parts: channel merging and channel decomposition. When the number of merged channels tends to infinity, polarization phenomenon will occur: one part of the channel will tend to a noiseless channel, and the other part will tend to a full-noise channel. The transmission rate of the noiseless channel will reach the channel capacity, while the transmission rate of the full noise channel tends to 0. Fig. 3 briefly illustrates the channel polarization process of Polar codes. The polarized subchannels are sorted by reliability, where the high reliability subchannels (lower noise) are used for transmitting user information as information bits; while the low reliability subchannels (higher noise) are designated as frozen bits, transmitting a predetermined value (usually 0) to aid in decoding. In a Polar code of length N, K of the most reliable subchannels are selected as information bits, while the remaining $N–K$ are frozen. This leads to a code rate of $R = K / N$.

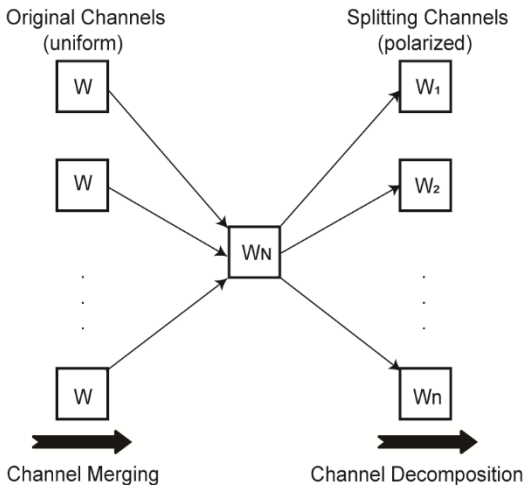

Fig. 3. Polar Codes Channel Polarization Process

The generator matrix of Polar codes is constructed recursively using the Kronecker product. For a code

length $N = 2^n$ (where $n \geq 1$), the core formula of the generator matrix is given as shown in (1) where $\mathbf{B}_N$ represents the bit reversal permutation matrix, which is used to reorder the input bits by performing a bit reversal operation on their indices.

$$\mathbf{G}_N = \mathbf{B}_N \cdot \mathbf{G}_2^{\otimes n}, N = 2^n, \mathbf{G}_2 = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}. \quad (1)$$

Due to the inherent characteristics of channel polarization and the recursive construction of the generator matrix, the code length N of Polar codes must be 2^n. As a result, Polar codes are less flexible in terms of code length compared to LDPC codes. In practical applications, shortening or puncturing techniques can be employed to adapt Polar codes to lengths that are not 2^n, but this typically results in performance degradation. The recursive construction of Polar codes makes the reliability of each sub-channel dependent on the decoding results of preceding channels. Since channel polarization is inherently a sequential process, the successive cancellation (SC) decoding algorithm becomes the most natural and efficient choice [17]. The SC decoding algorithm can be abstractly represented as a binary tree traversal. Fig. 4 illustrates the decoding tree for a Polar code ($N = 8$, $K = 4$). The tree contains of $1 + \log_2 N$ layers (including the root layer), and each layer i has 2^i nodes. Information bits and frozen bits are denoted by black and white circles. For each internal node in the tree, if both of its descendants have the same color, the node is marked with that color; otherwise, it is marked in gray. SC decoding leverages the information from already decoded bits to assist in making decisions for subsequent bits. It is simple to implement and well-suited for low-power scenarios. However, its main drawback lies in error propagation in short code blocks. Due to insufficient polarization of short code blocks, the reliability gap between channels is small, making it difficult for SC to effectively distinguish between good and bad channels. Once an error occurs, it tends to propagate along the decoding path, leading to further decoding failures. As a result, the BER tends to stagnate in the high SNR region.

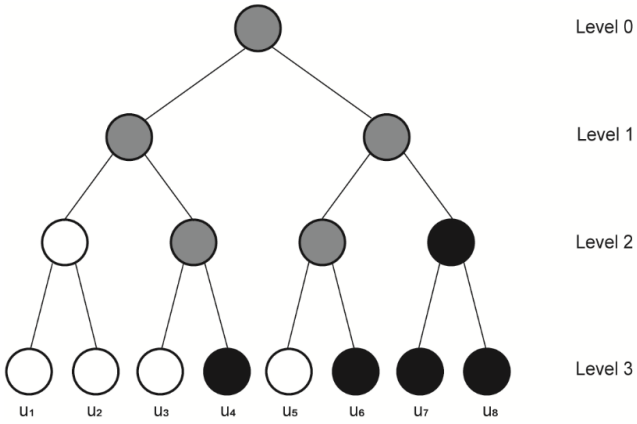

Fig. 4. Polar Code (N = 8, K = 4) Decoding Tree

In order to overcome the performance limitations of the basic SC algorithm in short code blocks, the Successive Cancellation List (SCL) and the Cyclic Redundancy Check-Aided Successive Cancellation List (CA-SCL) decoding algorithms have been proposed as improved solutions [18, 19]. The SCL algorithm maintains a list of candidate decoding paths (with a list size L) and expands up to L paths for each information bit, thereby reducing the impact of errors in any single decoding path. At the final stage, the most probable path is selected as the output, significantly enhancing error correction performance [18]. CA-SCL further integrates cyclic redundancy check (CRC) check bits during encoding, and during decoding, it prioritizes candidate paths that pass the CRC check. In the final selection, only the CRC-passing paths are considered, which further improves decoding accuracy [19]. In the 5G NR system, to meet the dual requirements of high reliability and short code length for control channels, CA-SCL algorithm is used for Polar-coded control information (https://portal.3gpp.org).

LDPC and Polar comparison in 6G

As the two most promising mainstream channel coding technologies for 6G, LDPC codes and Polar codes have made important progress in their respective fields. In this section, we discuss and analyze the development process of LDPC codes and Polar in 6G from four aspects: data throughput, error correction performance, decoding complexity and hardware implementation, flexibility and adaptive coding.

Data throughput

Channel coding in 6G communication system presents significant challenges due to the stringent power and energy efficiency constraints required to achieve Tbps throughput. As a key physical layer technology for achieving ultra-high-throughput, channel coding schemes must continue to evolve through innovations in code structure design, improvements in decoding algorithms, and more efficient hardware architecture in order to meet the stringent performance requirements of 6G. At present, significant progress has been made in achieving Tbps-level high-throughput decoding schemes for both LDPC and Polar codes. In the following, we provide a comparative analysis of the technical challenges and specific solutions related to realizing Tbps throughput for these two coding schemes.

Achieving Tbps-level throughput inevitably requires extensive parallel computation [20]. However, due to the recursive structure of channel polarization, Polar codes exhibit inherent sequential dependencies. Although SCL and CA-SCL decoding allow partial parallelism during path expansion and CRC checking, the core decoding process still requires sequential execution, thereby limiting the parallel decoding capability of Polar codes. In recent years, more high-speed Polar code decoder designs based on parallel architecture have

been proposed, including pipeline structures, partially parallel decoding and improved SC decoders [21–23]. These methods achieve higher throughput and reduce complexity in hardware implementation. The current Fast Polar code solution has achieved a data throughput of 1229 Gbps, meeting the throughput requirements of 6G [24]. The Fast Polar code solution improves decoding efficiency by optimizing the entire decoding tree architecture and hardware design.

The decoding algorithm of Fast Polar codes builds upon the Simple SCL (SSCL) framework [23, 24]. The SSCL decoding algorithm accelerates conventional SCL decoding by identifying 4 types of special nodes: Rate-0, Rate-1, Repetition (REP), and Single Parity Check (SPC). A Rate-0 node consists entirely of frozen bits, which are typically set to zero, while a Rate-1 node contains only information bits. A Rep node has all bits frozen except for the last one, which is an information bit. In contrast, an SPC node has only the first bit frozen, with the remaining bits serving as information bits [24]. Fig. 5 illustrates the decoding tree of a Polar code ($N = 32$, $K = 16$), which contains 4 types of special nodes. These special nodes enhance decoding efficiency by reducing recursive traversals, minimizing path expansions, and enabling parallel computation. As shown in Fig. 6, the decoding tree of Fig. 5 has been simplified by applying special node identification.

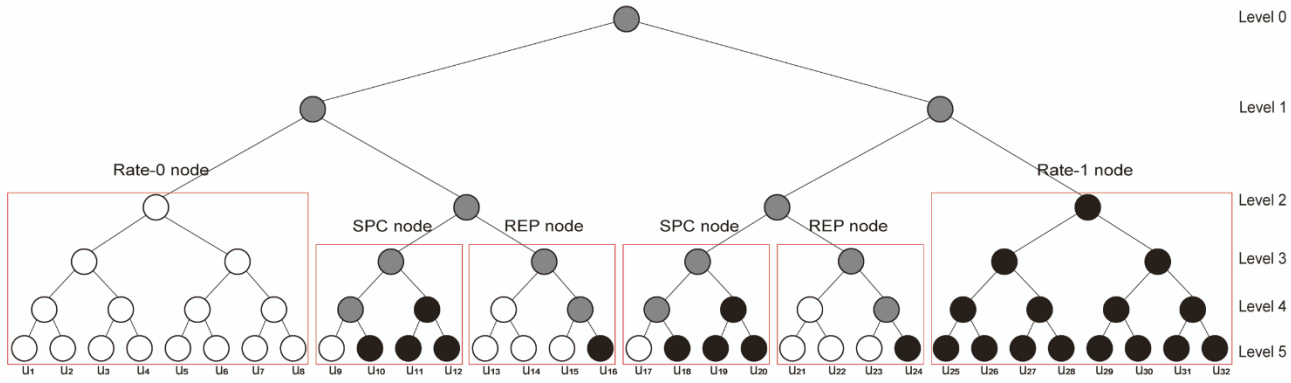

Fig. 5. Decoding Tree of a Polar Code (N = 32, K = 16) with 4 Types of Special Nodes

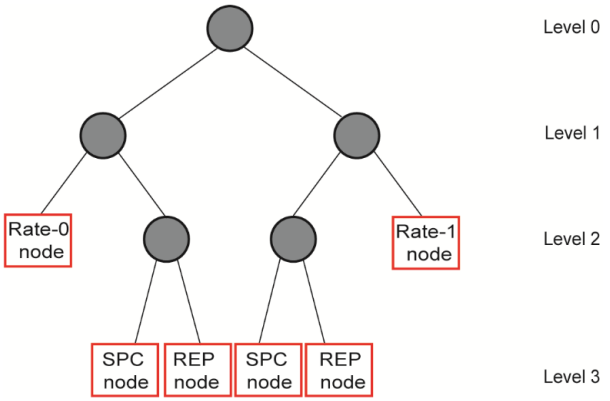

Fig. 6. Simplified Decoding Tree of a Polar Code (N = 32, K = 16)

The Fast SC decoding algorithm further extends 4 additional types of special nodes (subtree structures): dual-SPC (SPC-2) nodes, dual-REP (REP-2) nodes, repeated parity check (RPC) nodes, and nested parity check (NPC) for each type [24]. Then for medium-code-rate nodes that do not contain any of the 8 special node types, 2 extended Bose – Chaudhuri – Hocquenghem (BCH) codes are introduced to replace the original outer Polar code. By leveraging the superior minimum distance of BCH codes, this approach enhances error correction capability while also reducing decoding latency. Finally, by reallocating the code rate across the entire Polar code, all nodes reaching a certain size can be transformed into one of the 8 special node types or replaced with BCH codes, thereby maximizing the potential for fast decoding. The Fast SC decoding tree structure can be briefly represented as shown in Fig. 7. Such an approach significantly simplifies the decoding tree structure, greatly reducing the traversal depth, effectively avoiding the inefficient path processing overhead commonly encountered in conventional SCL decoders, thereby substantially improving decoding speed and laying the foundation for highly parallel decoding architectures. In hardware implementation, Fast Polar decoders commonly adopt a fully unrolled pipelined architecture combined with multiple dedicated processing elements, maximizing both parallel coverage of the decoding process and hardware resource utilization, thus supporting Tbps-level high-speed communication demands [24]. The unfolded decoder for Fast Polar codes implemented on 16 nm FPGA supports a code length of N=1024 and a code rate of $R = 0.875$. With a chip area of just 0.3 mm^2, it achieves an impressive data throughput of 1229 Gbps, reaching a breakthrough area efficiency of 4096 Gbps/mm^2.

Unlike Polar codes, LDPC codes, due to their sparse parity-check matrix structure and the characteristics of message-passing algorithms, can achieve efficient parallel decoding by enabling simultaneous operations on multiple nodes through the Tanner graph [9, 12, 25]. In

practical applications, the high parallelism of LDPC codes can cause multiple processing units to access the same nodes simultaneously, leading to data access conflicts and routing congestion, which ultimately degrade decoding performance [25]. The routing congestion problem in high-throughput LDPC decoders essentially arises from hardware resource contention caused by the parallel computation mode. By optimizing the decoding algorithms and hardware architectures, routing congestion can be alleviated, thereby maximizing hardware utilization. The row-based and column-based layered decoding algorithms group check nodes or variable nodes into layers, processing one layer at a time.

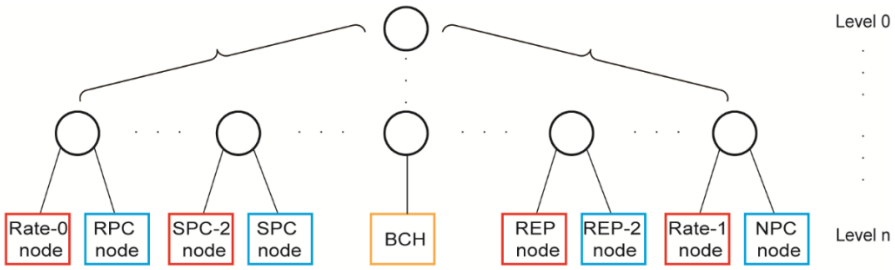

Fig. 7. Fast SC Decoding Tree with 8 Types of Special Nodes and BCH Codes

This decoding method is no longer fully parallel but partially parallel, yet it still significantly improves throughput while alleviating routing congestion issues [12, 25]. Currently, the highest-throughput LDPC decoder adopts a full-row layered decoding algorithm, combined with frame interleaving and multi-core techniques, achieving a data throughput of 860 Gbps [12]. The entire decoding process uses only a three-stage pipeline, where frame interleaving allows different frames' data to be interleaved and processed simultaneously within the pipeline, enhancing parallelism and hardware utilization while keeping the architecture simple. The above decoder adopts an 8-core parallel architecture implemented with 16nm ASIC technology, achieving 860 Gbps data throughput for the (1032, 860) LDPC code. It occupies a core area of 1.48 mm^2, resulting in an area efficiency of 581.1 Gbps/mm^2. Meanwhile, the decoder maintains flexibility in code rate, iteration count, early stop, and suitable for (1–2K) medium length LDPC codes. The current highest throughput decoding solutions for Polar and LDPC codes are compared in Table 1.

TABLE 1. Comparison of Highest Throughput Decoders for Polar and LDPC Codes

Parameter	Polar codes	LDPC codes
Throughput (Gbps)	1229	860
Algorithm	Fast Polar	Layered
Decoding architecture	Fully unrolled pipelined dedicated processing elements	Multi-core full-row parallel layered frame interleaving
Code length	1024	1032
Code rate	7/8	5/6
Technology	16 nm FPGA	16 nm ASIC
Frequency (MHz)	1200	1000
Core area (mm2)	0.30	1.48
Area efficiency (Gbps/mm2)	4096	581.1
Energy efficiency (pJ/bit)	0.63	3.24
Supported code lengths	Fixed	(1–2k)
Supported code rates	Fixed	Flexible code rate

As shown in Table 1, the data throughput of Polar codes is significantly higher, primarily due to the extremely unfolded pipelined design. However, leading in throughput does not imply comprehensive superiority; the Polar solution achieves its throughput at the cost of extremely high resource consumption. The Fast Polar decoder fully unfolds the entire Polar decoding tree, assigning a dedicated computational unit to each node for maximum parallelism. As code length increases, the required logic gate count grows exponentially, severely constraining practical applications. In reality, Polar codes can only be implemented with limited lengths – longer codes (more than 10000 bits) become impractical. This approach is highly customized, supporting only fixed code lengths and code rates. Any changes in communication standards or application requirements necessitate complete hardware redesign, making large-scale production challenging. In real world communication systems, channel coding needs to dynamically adapt to different scenarios, and the lack of flexibility is a major drawback. In contrast, LDPC decoding solutions achieve a better balance between high-throughput, and flexibility. Although its multi-core architecture enhances performance, it also incurs substantial hardware resource consumption, potentially limiting deployment in resource-constrained applications. In summary, if extreme throughput and energy efficiency are the priority and resources are abundant, the fully unfolded Polar solution is a good choice. However, if usability, flexibility, and scalability are more critical, the multi-core LDPC architecture is clearly the more practical and rational option.

Error correction performance

The error correction performance of both LDPC and Polar codes improves significantly as the code length increases, but their optimization mechanisms differ. LDPC codes benefit from the increased structural flexibility of the parity-check matrix, enabling the construction of sparse matrices with larger minimum girth, which effectively reduces the error floor [26]. In contrast, Polar codes rely on the channel polarization effect; as the code length N increases, the proportion of reliable subchannels K/N approaches the channel capacity C, theoretically enabling performance close to the Shannon limit [17]. Under short code length conditions, LDPC codes suffer from increased error floors due to limited sparsity and smaller girth, while Polar codes experience a decline in error correction capability due to incomplete channel polarization and a higher number of unreliable subchannels. In addition to code length and structure, the choice of decoding algorithm also significantly impacts the error-correcting performance of LDPC and Polar codes. Generally speaking, more advanced and complex decoding algorithms provide better error correction performance [27, 28].

In the 6G system, the error correction performance of LDPC and Polar codes continues to evolve to meet the demands of ultra-large-scale data transmission and ultra-high reliability, and is constantly optimized for their respective applicable scenarios. For LDPC codes, in order to improve the base matrix design, a graph theoretic method based on edge coloring has been proposed. In the construction of codes, this method analyzes the edge coloring properties of the VN graph to identify specific 6-cycle and 8-cycle structures that should be avoided in the exponent matrix. By effectively eliminating the occurrence of 8-cycles, the code performance is enhanced and the error floor is significantly reduced [26]. At the same time, to improve the performance of layered decoding algorithms, analyzing the trapping sets layer profile and optimizing the layer update order can effectively reduce the error floor of LDPC decoders and enhance error-correcting capability [27]. Additionally, to improve performance in short code length scenarios, generalized LDPC codes have been proposed, in which some of the single parity check nodes in traditional LDPC codes are replaced with more powerful generalized constraint nodes (such as BCH codes). Combined with optimized decoding algorithms, this approach improves error correcting performance and decoding efficiency in short block lengths, surpassing Polar codes and CA-SCL decoding schemes [29]. For Polar codes, to further enhance performance in short code length, Parity-Check-Concatenated Polar Codes have been proposed. By introducing parity-check codes outside the Polar code structure and leveraging their flexible design with distributed layout characteristics, this approach helps the SCL decoder effectively detect and prune error paths [30], thus demonstrating enhanced error correction capability in short-code and low-code-rate scenarios. Improvements to the decoder include two methods aimed at leveraging the error correction capability of CRC to enhance the decoding performance of Polar codes under short code length conditions [28]. Error-Correcting Table based segmented CA-SCL decoder introduce segmented CRC checks and pre-constructed error lookup tables to enable efficient identification and correction of local errors, thereby improving overall decoding performance. Deep Learning based segmented CA-SCL decoder leverages deep learning models to automatically learn complex error patterns and combines them with segmented CRC for dynamic path adjustment and error correction, thus enhancing decoding accuracy, robustness, and adaptability [28].

Overall, the development direction for 6G LDPC codes focuses on achieving efficient error correction performance across both long and short code length scenarios by enhancing girth, eliminating the effects of trap sets and optimizing short codes structures, while Polar codes, through structural and decoder optimization, have enhanced its performance advantage in short code length, demonstrating stronger competitiveness in control signaling and small data packet high-reliability transmission.

Decoding complexity and hardware implementation

LDPC codes employ message-passing-based iterative decoding algorithms, such as the belief propagation (BP) algorithm, the min sum (MS) algorithm, and their improved variants [31, 32]. The core idea of message passing is to progressively refine the estimation of the codeword through information exchange between VNs and CNs. The typical decoding complexity of LDPC codes is $O(Nd_cI)$ where N is the code length, d_c is the check node degree, and I is the number of iterations. O represents the scaling trend of decoding complexity, but since the computational load for a single message update operation differs across algorithms, the actual complexity must be multiplied by a different constant. In Polar code decoding, the SC algorithm processes each bit by traversing a tree of depth $\log N$, resulting in an overall complexity of $O(N\log N)$ for N bits [17]. The SCL algorithm enhances SC by maintaining L decoding paths. The increased complexity in SCL comes from path extension, metric calculation, and pruning, raising the total complexity to $O(LN\log N+LN\log L)$ [18]. CA-SCL further adds a CRC check on top of SCL. For each of the L candidate paths, a CRC check with complexity $O(m)$ (where m is the CRC length) is performed. Therefore, the CRC stage adds $O(Lm)$ to the overall cost, resulting in a final CA-SCL decoding complexity of $O(LN\log N+LN\log L+Lm)$ [18, 19]. Generally, higher-order decoding algorithms exhibit higher computational complexity and superior decoding performance. However, theoretical performance should not be the sole focus; the feasibility and efficiency of hardware implementation must also be carefully considered.

In practical applications, LDPC and Polar codes face different challenges in hardware implementation. LDPC decoding relies heavily on parallel and iterative computations, which generate a large volume of intermediate data, often leading to routing congestion and significantly increasing memory resource requirements [6, 33]. In contrast, Polar codes typically employ SCL and its enhanced decoding algorithms, which require tracking multiple decoding paths simultaneously. Each path must independently store its intermediate states, resulting in significant implementation challenges in multi-path memory management, path sorting, and parallelization within the recursive decoding structure [18, 34, 35]. LDPC codes can reduce the routing complexity of decoders by optimizing the interconnect structure between nodes. Simultaneously, strategies such as layered decoding and phased update mechanisms can effectively mitigate computational resource contention and routing congestion [12, 25, 33]. Building on this, the introduction of multi-level storage architectures and intelligent data scheduling mechanisms enables most data flows to be processed locally, significantly reducing long distance cross module transfers and routing resource consumption, while avoiding redundant data access, computation, and storage operations [36]. These techniques significantly reduce hardware resource consumption while meeting high-throughput demands, making LDPC codes especially suitable for 6G communication systems where both energy efficiency and throughput are critical.

SCL decoding algorithms and their variants can dynamically eliminate redundant paths through techniques like path merging and pruning, thereby reducing the number of paths that need to be managed and stored during decoding [34, 35]. Additionally, by integrating node-level parallel processing, unfolded hardware implementations of recursive structures, and pipeline optimization strategies, higher data throughput and efficient utilization of hardware resources can be achieved while ensuring decoding performance [22, 24]. The main practical issues of LDPC and Polar codes, along with their corresponding solutions in decoding algorithms and hardware optimization, are given in Table 2.

TABLE 2. The Main Application Challenges of LDPC and Polar Codes, and Their Solutions in Decoding Algorithms and Hardware Optimization

Aspects	LDPC codes	Polar codes
Main hardware challenges	High storage resource consumption, routing congestion, resource contention	Large multi-path storage overhead, complex path sorting management, recursive structure hinders parallelism
Algorithm optimization strategies	Layered decoding, partial update, optimized Tanner graph connectivity	Path pruning and merging, simplified path splitting, node-level parallelism
Hardware optimization methods	Multi-level memory hierarchy, intelligent data scheduling, localized memory access, module reuse and compute / data separation	Unrolled recursive structure, pipeline structure design, compressed storage and path reuse

In conclusion, a more rational decoding algorithm design can significantly alleviate common challenges encountered in hardware deployment. By combining hardware-oriented structural optimization and efficient implementation strategies, it is possible to not only improve overall decoding efficiency but also reduce area and power consumption while meeting performance requirements, thereby achieving a communication system design with higher engineering feasibility.

Flexibility and adaptive coding

The communication environment in 6G systems is more complex and dynamic, requiring channel coding schemes to possess a high degree of flexibility and adaptability. Flexibility refers to the ability of a coding scheme to support various code lengths, code rates, and hardware implementation architectures, serving as the foundation for adaptability. Adaptability refers to the capability of the coding scheme to dynamically adjust its parameters based on real-time channel conditions, user demands, and resource availability.

As the two mainstream channel coding schemes, LDPC codes and Polar codes demonstrate different strengths and application scopes in terms of flexibility and adaptability due to their structural design differences. LDPC codes, owing to the sparse structure of their parity-check matrices, exhibit excellent performance in terms of flexibility and adaptability [32, 37]. Through flexible configuration of matrix structures, LDPC codes support a wide range of code lengths and code rates, accommodating various modulation schemes and spectrum configurations. This enables effective support for dynamic spectrum access and elastic resource scheduling [38]. At the hardware level, the quasi-cyclic structure of LDPC codes facilitates modular hardware design, enhancing hardware reusability and allowing flexible parameter adjustment based on service requirements. This endows encoder and decoder architectures with dynamic reconfiguration capabilities [37, 38]. In terms of adaptability, LDPC codes utilize mechanisms such as puncturing, repetition, and rate matching to flexibly adjust the effective code rate under dynamic channel conditions [38, 39]. In HARQ schemes, LDPC codes support incremental redundancy retransmission and soft information accumulation decoding, significantly improving link reliability and transmission efficiency [40]. Furthermore, LDPC codes have the ability to dynamically optimize the decoding process based on channel conditions. By adding a small amount of logic and memory overhead, the maximum number of decoding iterations can be

adaptively adjusted according to the channel state, achieving an optimized balance between decoding performance and computational complexity [41].

Compared with LDPC codes, Polar codes exhibit certain limitations in terms of flexibility, as their code length must be 2^n [17, 42]. This constraint compromises both the efficiency and performance of traditional construction methods when dealing with codewords whose lengths are not 2^n, thus limiting their suitability for large-scale, dynamic resource allocation scenarios [42]. To overcome the limitations of traditional Polar codes in terms of flexibility, researchers have proposed various enhancement strategies. Firstly, at the code construction level, general construction techniques such as universal frozen bit interpolation and simulation-driven codeword optimization have been introduced. These methods reduce reliance on specific channel models, thereby improving the applicability of Polar codes across diverse channel conditions [43–45]. Secondly, to address the original design constraint of Polar codes supporting only code lengths that are 2^n, researchers have developed variable-length techniques such as puncturing and shortening, enabling encoding for arbitrary frame lengths [46, 47]. In terms of adaptability, Polar codes have also shown progressive improvements. By dynamically selecting frozen bit positions, pruning decoding paths, and adjusting decoding depth, Polar codes can optimize the decoding process in real time according to channel quality [48, 49]. Moreover, some studies have introduced AI-based mechanisms for path selection, aiming to achieve intelligent and channel-aware adaptive optimization [28].

6G long and short code block channel coding selection

6G communication scenarios are expected to exhibit an unprecedented diversity of requirements. On one hand, the growing demands of high-throughput services such as 4K/8K video, XR, and holographic communications are driving the evolution of 6G channel coding toward longer, high-capacity codes capable of supporting Tbps-level data streams with enhanced robustness. Accordingly, code lengths are expected to exceed 10000 bits [6] (https://hexa-x-ii.eu/wp-content/uploads/2024/04/Hexa-X-II%20D4%203%20v1.0%20final.pdf). On the other hand, scenarios such as IoT cluster communication, control signaling, semantic communications, and V2X frequently involve small data packets, instantaneous response, and low-complexity constraints, which drive coding technologies to further optimize toward ultra-short code lengths (such as less than 128 bits) [50, 51]. The evolution trends in code lengths for 6G channel coding are summarized in Table 3.

TABLE 3. Comparison between Long and Short Code Design Considerations in 6G Channel Coding

Aspects	Long code	Short code
Code length range	> 10000 bits	< 128 bits
Application scenarios	Holographic communications, 4 K / 8 K video, XR entertainment	V2X, IoT cluster communication, semantic communication, control signaling
Performance characteristics	High error correction capability, near capacity performance, high parallelism	Low latency, low complexity, fast decoding
Deployment characteristics	Rich computing resources (e.g., base stations, edge servers)	Resource-constrained nodes (e.g., terminals, sensors)

The stringent requirements for both long and short codes in 6G communications have spurred extensive research on LDPC and Polar codes. In general, implementing high-throughput decoders for short codes is relatively easier than for long codes, as they require less memory, simpler wiring and control logic, and are more amenable to parallel and pipelined processing. Conseq11uently, short code decoders are more likely to achieve both high throughput and low latency in practical hardware deployments. By contrast, although long codes offer higher coding gains and better error performance, their decoder design and hardware implementation still face a number of technical challenges. For LDPC codes, increasing the code length leads to a more complex parity-check matrix, resulting in excessive interconnect usage, routing congestion, and clock closure difficulties in hardware implementation [25, 52]. Moreover, the iterative decoding process involves a large number of parallel node updates and message exchanges across thousands of edges, placing heavy demands on computational resources and memory bandwidth [53]. These factors degrade the iteration speed and further exacerbate latency and power consumption constraints. Currently, SC-LDPC codes can significantly alleviate the aforementioned implementation challenges due to their favorable structural characteristics, thereby enabling the design of high-throughput decoders for long code applications [33, 52]. Polar codes, on the other hand, demonstrate excellent performance in short code scenarios – particularly when employing SCL and its variants as decoding algorithms. However, in long code regimes, they face notable limitations. Due to the bit serial nature of the Polar codes structure, parallelism is limited; as the length N and list size L increase, the overhead of path management, metric updating and sorting, and LLR/partial-sum accesses in SCL decoding grows accordingly [17, 54], making it more challenging to realize hardware with both high throughput and low latency for long codes [18, 55]. As a result, there is currently a lack of landmark

hardware implementations for high-throughput decoders targeting long Polar codes. Table 4 summarizes the comparison of LDPC codes and Polar codes from different perspectives of high-throughput decoding schemes for long code length.

TABLE 4. Simplified Comparison: Long-Length LDPC vs. Polar Codes in High-Throughput Implementation

Aspects	LDPC	Polar
Structure	Large-scale parity matrix, routing congestion	Deep decoding tree, hierarchical dependencies
Decoding	Iterative, parallel message passing	Serial SC/SCL, bit-wise dependency
Resources	High compute and memory bandwidth	Exponential path/memory growth
Throughput	Limited by iteration and interconnect	Hard to parallelize, low throughput
Feasibility	Mature hardware solutions (e.g., SC/QC-LDPC)	No high-throughput long-code implementations

In practical applications, it has been observed that, apart from SC-LDPC codes, most other coding schemes are restricted to short block lengths when targeting Tbps-level throughput [52, 56, 57]. In contrast, SC-LDPC codes, owing to their spatially coupled, stream-like (semi-infinite) structure, can theoretically support extremely long block lengths without compromising decoder throughput.

The process of constructing a (3, 6, 2, *L*) SC-LDPC code coupling chain is as follows: Fig. 8a is a (3, 6) regular LDPC code protomodule graph with the basis matrix **B** = [3 3], and Fig. 8b is the *L* identical but mutually uncorrelated LDPC code protomodule graphs. Then, the *L* mutually uncorrelated LDPC code original modal graphs are connected according to the edge expansion rule to obtain a SC-LDPC code coupling chain, as shown in Fig. 8c.

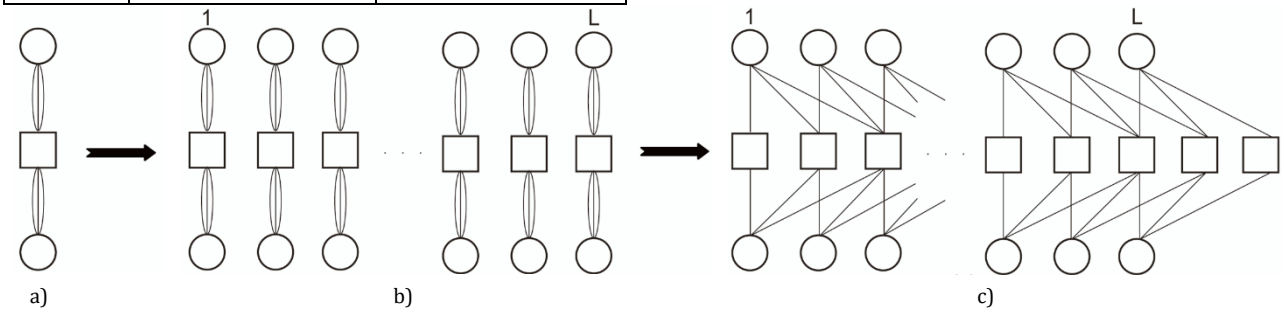

Fig. 8. The Construction Process of SC-LDPC Code Original Modal Map

Their architecture enables the chaining of multiple sub-decoders, each operating on smaller, localized sub-blocks in a pipelined manner. This architectural advantage makes SC-LDPC particularly suitable for Tbps-class decoder implementations in next-genera-tion systems [33, 52]. The decoder architecture based on the fully parallel window decoding (FPWD) mechanism is the first SC-LDPC decoder capable of achieving a throughput exceeding 100 Gbps [33]. In this architecture, multiple window decoders operate fully in parallel, each independently processing a segment of the code-word, which significantly enhances decoding concurrency. To support high-throughput data streams, a custom interconnect network is implemented, and the CN and VN processors are optimized through pipelining to eliminate data dependency bottlenecks. Additionally, by introducing register reuse and efficient message update mechanisms, the system achieves a throughput of 336 Gbps (operating at 700 MHz) using the 22 nm FD-SOI process for an SC-LDPC code with a length of 51328, a sub-block size of 640, and a coupling width of 1. However, the architecture supports only fixed code lengths and rates, which limits its flexibility for dynamic or adaptive communication scenarios.

With the advancement of system-on-chip (SoC) technology, there remains significant potential to further improve data throughput. A key challenge is achieving high throughput while supporting diverse code rates and lengths to address varied communication needs. Recent developments in SC-LDPC codes have demonstrated notable improvements inflexibility [58, 59]. Traditional SC-LDPC codes are typically constructed by applying edge spreading to a predefined LDPC block code, which inherently limits the design space due to structural constraints. In contrast, Edge-Spreading Raptor-Like (ESRL) SC-LDPC codes are free from such dependencies and directly target the optimization of the coupled matrix from the ground up [58]. This design philosophy introduces structural asymmetry, providing greater flexibility in constructing the coupled protograph. The ESRL code structure is described by the triplet **B**, **T**, **Q**, **B** is the uncoupled protograph, **T** is the edge-spreading matrix, and **Q** is the tail matrix. By enabling flexible tail matrix pruning, ESRL codes support continuously adjustable code rates, making them particularly well-suited for dynamic service requirements in 6G scenarios. Under the same hardware conditions, ESRL architecture achieves significantly higher throughput than conventional 5G-NR LDPC codes, reaching 209.4 Gbps with a maximum block length of 23790 bits.

SC-LDPC codes, with their unique structure, remain one of the most promising solutions for achieving Tbps-

level throughput in long block length scenarios, demonstrating excellent parallelism and hardware adaptability [33, 52, 58]. Although LDPC codes offer excellent performance and high parallelism in long code scenarios, their performance significantly degrades in short code applications. In such cases, short cycles are more likely to form in the Tanner graph, leading to poor iterative convergence, increased error propagation, and the emergence of error floors. Moreover, LDPC decoders typically consume substantial hardware resources, have low efficiency when processing short packets, and exhibit poor overall energy efficiency.

Polar codes also face certain challenges in short code scenarios, such as insufficient polarization, latency due to their inherently sequential decoding structure, and increased hardware complexity caused by multipath decision processing. However, these issues can be mitigated by introducing CA-SCL decoding to enhance path selection reliability [19], applying Fast-SSCL architectures to accelerate decoding, and utilizing path merging and sorting optimizations to reduce computational redundancy and hardware costs [60]. As a result, Polar codes have achieved a favorable balance between performance and efficiency in short-code control signaling in 5G systems. Building on the adoption of Polar codes for control signaling in 5G, short-code design in 6G is expected to further pursue ultra-low latency, ultra-low power consumption, and dynamic adaptability [61, 62]. New approaches may include enhanced CRC-aided optimization and neural network-based coding schemes to meet the increasing complexity and granularity of control signaling requirements [63]. Ultimately, the goal is to achieve low-complexity, highly reliable coding mechanisms for ubiquitous communication, thereby supporting the intelligent network infrastructure of 6G.

Uniform channel coding framework

Given that the 3GPP has yet to finalize the channel coding standard for 6G, both academia and industry are actively exploring the feasibility of a unified coding framework [64]. It is important to note that “unified” does not necessarily imply the use of a single channel code [64–66]. A unified coding framework can follow two main approaches (1) employing a single channel code to cover all scenarios, or (2) constructing a flexible platform capable of dynamically switching between or combining multiple coding schemes.

The first approach aims to develop a highly scalable universal channel code capable of covering a wide range of communication scenarios – from ultra-short to long packets, and from ultra-low latency to ultra-high throughput. A prominent example in this direction is the Generalized LDPC with Polar-like Components (GLDPC-PC) code, which combines the sparsity of LDPC codes with the structural properties of Polar codes [66]. Simulation results have shown that GLDPC-PC can outperform 5G LDPC codes by approximately 0.3 dB at a BER of 10^{-4} under medium code lengths (1024–8192 bits), while also reducing the number of decoding iterations by about half to one-third. This makes GLDPC-PC a promising candidate for a unified coding framework in 6G. However, its robustness and scalability for extreme short-code (< 128 bits) and long-code (> 10k bits) scenarios still require further investigation.

The second approach in the pursuit of multi-code-cooperative unified FEC architectures is exemplified by three recent works, which reflect distinct but complementary strategies toward this goal: model-level abstraction via neural networks, instruction-level programmability, and full hardware-level integration [65, 67, 68]. First, the Unified Error Correction Code Transformer (UECCT) introduces a transformer-based, code-agnostic neural decoder capable of simultaneously decoding multiple linear block codes (LDPC, Polar, BCH) within a single architecture [65]. This work establishes a new model-level unification paradigm based on deep learning, offering enhanced flexibility and scalability for AI-native 6G receivers. It is particularly well-suited for short-packet communications, control channels, and intelligent edge applications. At the microarchitectural level, multi-mode platforms such as the Quad-mode Forward Error Correction Application-Specific-Instruction-set Processor (QFEC ASIP) propose a software-defined decoder supporting LDPC, Polar, Turbo, and convolutional codes [67]. QFEC offers a compelling programmable decoding solution with excellent area and energy efficiency, suitable for SoCs and software-defined radio (SDR) platforms in heterogeneous network environments. Finally, at the hardware integration level, a chip-level solution supports LDPC, Polar, Turbo, and convolutional codes under a unified data path and memory system [68]. This design represents the hardware-level convergence of multiple decoding logics and resources, effectively addressing scalability bottlenecks in large structured codes and enabling real-time decoding for 6G transceivers. The development status of these three types of multi-code cooperative frameworks is summarized in Table 5. Those research works collectively demonstrate that multi-code cooperative frameworks is a viable route toward 6G FEC unification. The direction forward lies in cross-layer co-design that enables adaptability, reuse, and efficiency across multiple abstraction levels. However, such cooperation also introduces overheads in design complexity, scheduling, and memory management, which may limit scalability in real-time applications. Moreover, while these solutions achieve decoder-level integration, full stack-level convergence – particularly in link adaptation and cross-layer control – remains an open research challenge.

TABLE 5. Development Status of These Three Types of Multi-Code Cooperative Frameworks

Layer	Representative Work	Key Innovation
Model	UECCT	Transformer-based neural decoder with shared logic
Micro-architecture	QFEC ASIP	Instruction-level decoder with mode reusability
Hardware SoC	Fully Configurable Decoder	Unified data path, compression, quad-mode chip

Challenges and future directions

In 6G systems, both LDPC and Polar codes face significant challenges related to computational complexity, which becomes increasingly critical given the rising demands for ultra-high data rates and ultra-low latency. Efficient hardware implementation is another pressing issue, especially in largescale, resource-constrained 6G deployments. One of the core challenges is to strike a balanced trade-off among error correction performance, energy efficiency, and decoding latency, ensuring that these channel coding techniques can adapt to diverse and dynamic application scenarios.

Looking ahead, LDPC and Polar codes are expected to increasingly integrate with AI techniques to enable intelligent adaptation and optimization. By leveraging channel state information and historical data, AI-assisted encoders and decoders can dynamically adjust parameters to optimize performance under varying channel conditions. Additionally, the use of general-purpose processors such as GPUs can facilitate structural optimization and decoding acceleration. Specifically, GPUs can help optimize interconnect topologies for LDPC codes and enhance path selection strategies for Polar codes, ultimately improving energy efficiency and boosting overall throughput. These directions represent promising pathways toward making LDPC and Polar codes more robust, flexible, and scalable for future 6G communication systems.

Conclusions

In the paper, we analyze the development status of LDPC and Polar codes in the context of 6G communication, with particular focus on the design considerations for long and short code blocks. Significant progress has been made in achieving Tbps-level throughput for short codes, where Polar codes demonstrate outstanding decoding efficiency and energy performance. However, LDPC codes offer superior flexibility and adaptability, making them more favorable in dynamic communication environments.

For long block length scenarios, SC-LDPC codes maintain a strong advantage due to their structured parallelism and hardware scalability. In contrast, polar codes face limitations stemming from their sequential decoding nature, channel polarization dependency, and implementation challenges at large code lengths.

Importantly, we emphasize that the evolution of 6G channel coding should not be viewed as a competition between LDPC and Polar codes, but rather as a path toward coexistence and potential integration. The emergence of unified frameworks – such as GLDPC-PC codes, AI-assisted decoding strategies, and reconfigurable multi-mode platforms – indicates a promising direction for designing adaptive and efficient FEC architectures capable of meeting the diverse demands of 6G systems.

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Статья поступила в редакцию 31.08.2025; одобрена после рецензирования 29.09.2025; принята к публикации 30.09.2025.
The article was submitted 31.08.2025; approved after reviewing 29.09.2025; accepted for publication 30.09.2025.

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Авторы сообщают об отсутствии конфликтов интересов.
The authors declare no conflicts of interests.